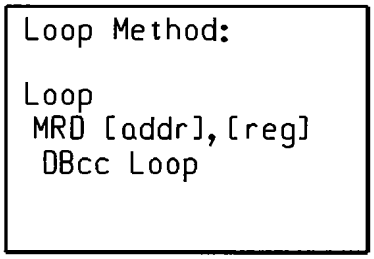

Fig. 1A
PRIOR ART

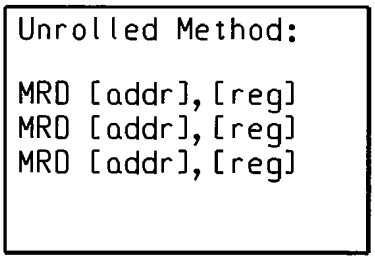

Fig. 1B
PRIOR ART

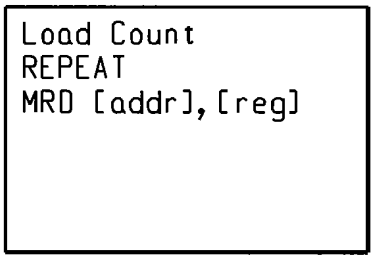

Fig. 2

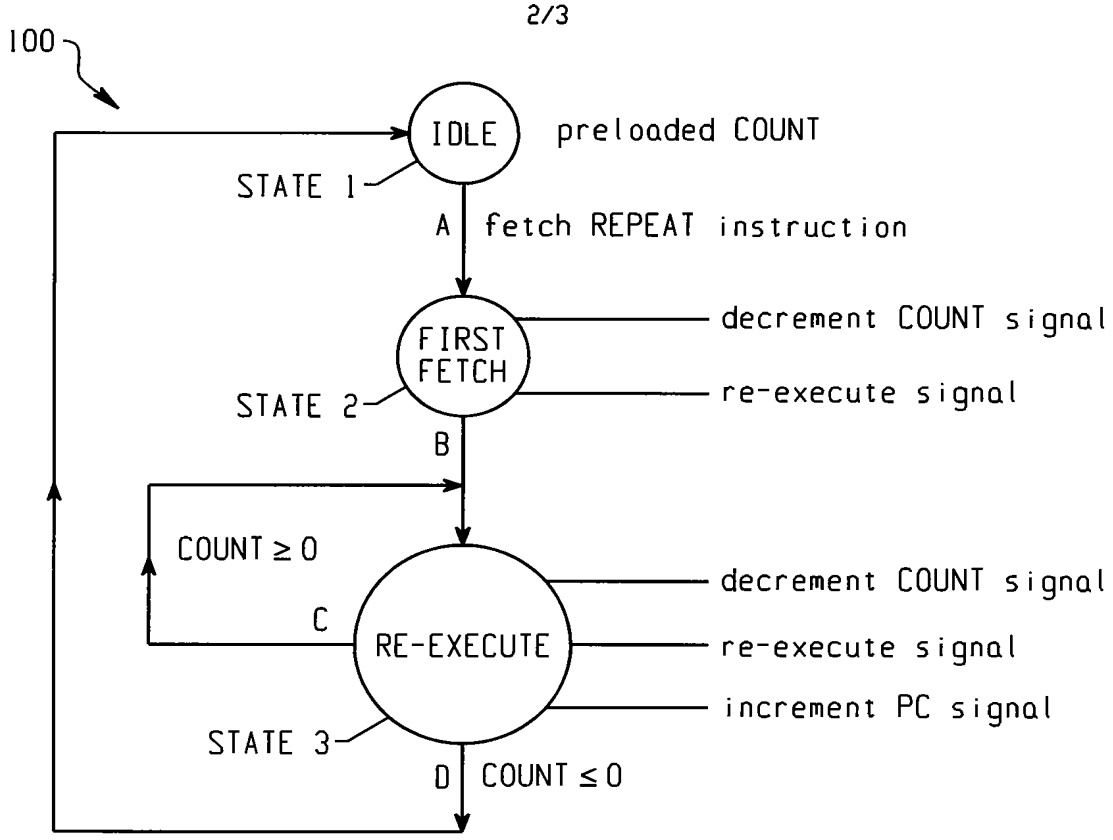

Fig. 3

PROGRAM COUNTER (PC)	TRANSITION	OPERATION
x10	A	fetch REPEAT instruction
x11	B	fetch instruction to be repeated ($INST_R$)
x11	C	execute $INST_R$
x11	C	execute $INST_R$
x11	C	execute $INST_R$
x11	C	execute $INST_R$
x11	C	execute $INST_R$
x12	D	fetch next instruction

Fig. 4

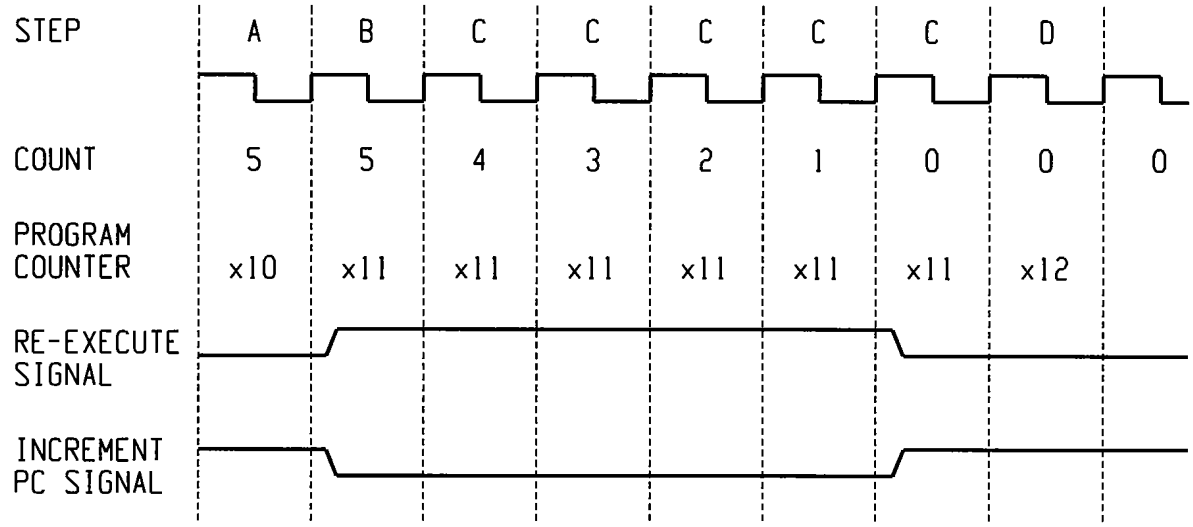
STEP
A
B
C
C
C
C
C
D
COUNT
5
5
4
3
2
1
0
0
0
PROGRAM COUNTER
x10
x11
x11
x11
x11
x11
x11
x12
RE-EXECUTE SIGNAL
INCREMENT PC SIGNAL

Fig. 5

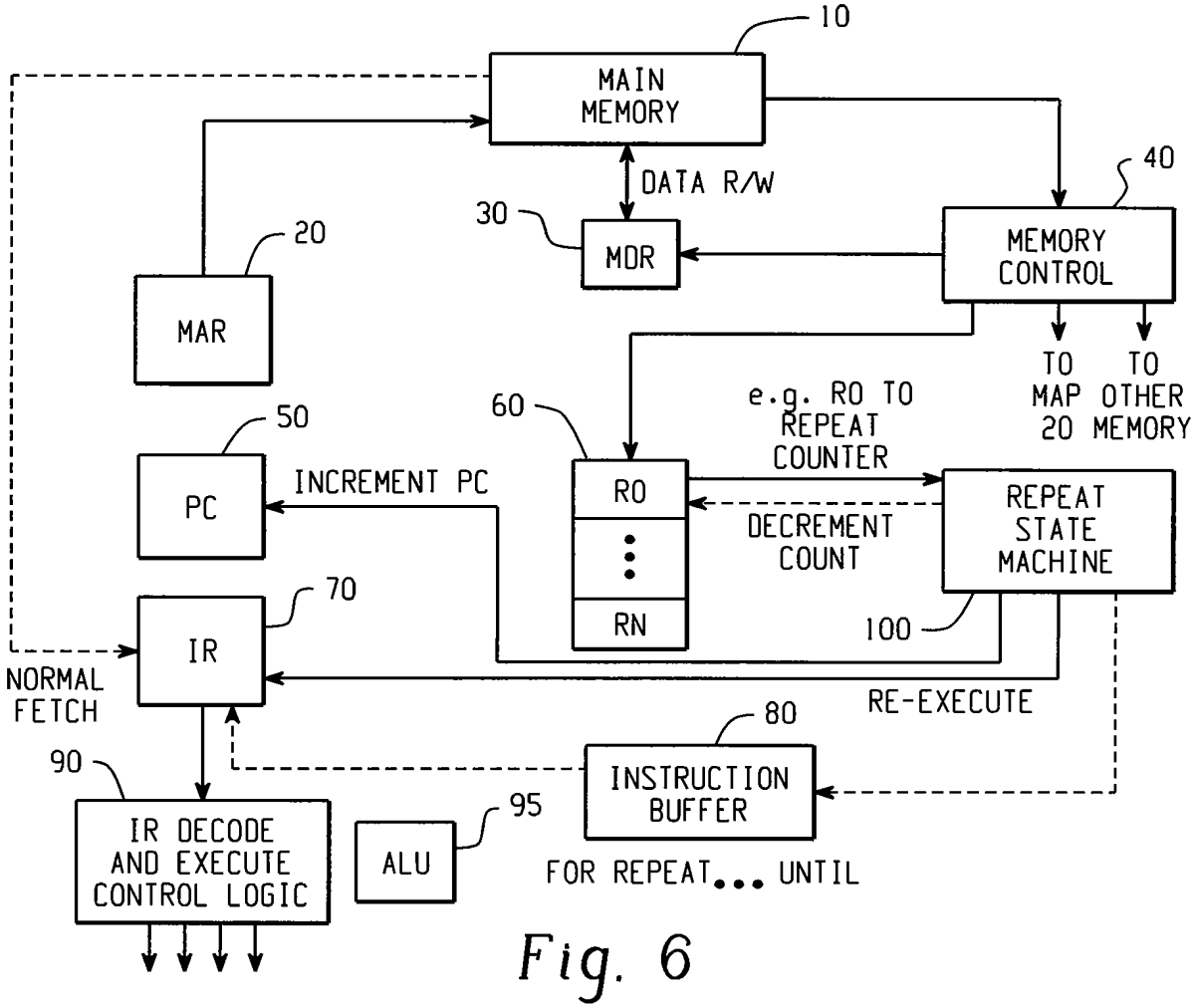
10
MAIN MEMORY
DATA R/W
40
30
MDR
MEMORY CONTROL
20
MAR
TO MAP 20
TO OTHER MEMORY
60
e.g. R0 TO REPEAT COUNTER
50
PC
INCREMENT PC
R0
RN
DECREMENT COUNT
REPEAT STATE MACHINE
70
IR
100
NORMAL FETCH
RE-EXECUTE
80
INSTRUCTION BUFFER
90
IR DECODE AND EXECUTE CONTROL LOGIC
ALU
95
FOR REPEAT... UNTIL

Fig. 6